IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	Docket No.: **TI-34776**
Khurram Muhammad	Art Unit: **2816**
Serial No.: **10/712,593**	Examiner: **Le, Dinh Tranh**
Filed: **11/13/2003**	Conf. No.: **8991**

For: **A TECHNIQUE FOR IMPROVING ANTIALIASING AND ADJACENT CHANNEL INTERFERENCE FILTERING USING CASCADED PASSIVE IIR FILTER STAGES COMBINED WITH DIRECT SAMPLING AND MIXING**

LETTER PROPOSING DRAWING AMENDMENT UNDER RULE 123

Commissioner for Patents

Alexandria, VA 22313-1450

MAILING CERTIFICATE UNDER § 37 CFR 1.8(a)

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Commissioner for Patents and Trademarks, Alexandria, VA 22313-1450 on **August 17, 2005**.

Elizabeth Austin

Dear Sir:

Responsive to the Examiner's request for clarification, Applicants propose amending drawing Figures 2, 3, 5 and 6, as set forth below.

Regarding Figure 1, Applicants propose adding the identifier "Output" and a lead line to the source of transistor S_2. Support for the amendment and is enabled by the specification and derived from US 2003/0035499 A1 which was incorporated by reference.

Regarding Figure 2, Applicants propose adding the identifier "LO" to the gate of the transistor below "FIG. 2". Applicants also propose adding a DCU (Digital Control Unit) that outputs control lines for the switches. Support for the amendment is shown in Figure 4A which shows the DCU. The timed operation of switches to combine and split capacitors is described in the specification. LO is shown in Figure 4A and in US 2003/0034499 A1, which is incorporated by reference.

Regarding Figure 3, Applicants propose adding the identifier "LO" to the gate of the transistor just to the left of the identified "BANK 2". Applicants also propose adding an identifier "TO IFA" and a lead line from the identified to node "C". Applicants further propose adding a DCU (Digital Control Unit) that outputs control lines for the switches. Support for the amendment is shown in Figure 4A which shows the DCU. The timed operation of switches to combine and split capacitors is described in the specification. LO is shown in Figure 4A and in US 2003/0034499 A1, which is incorporated by reference. The output connected to IFA input is described on page 6: line 16 in the specification.

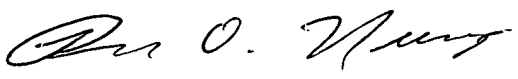
Regarding Figure 5, Applicants propose adding the identifier "LO" to the gate of the transistor just to the left of the identified "BANK 2". Applicants also propose adding the identified "CTL_SAZ" to the gate of the transistor just above the identified "BANK 2". Applicants further propose adding the identifier "CTL_SBZ" to the gate of the transistor just above the identifier "BANK 1". Applicants yet further propose adding an identifier "TO IFA" and a lead line from the identified to node "B". Applicants also propose adding a "Clock Generation" box with identified output signals CTL_SAZ, CTL_SBZ, CTL_D, and CTL_P. The timed operation of switches to combine and split capacitors is described in the specification on page 6, lines 17-29. LO is shown in Figure

4A and in US 2003/0034499 A1, which is incorporated by reference. The output connected to IFA input is shown also in Figure 4B.

Regarding Figure 6, Applicants propose adding the identifier "LO" to the gate of the transistor just to the left of the identified "BANK 2". Applicants also propose adding the identified "CTL_SAZ" to the gate of the transistor just above the identified "BANK 2". Applicants further propose adding the identifier "CTL_SBZ" to the gate of the transistor just above the identifier "BANK 1". Applicants yet further propose adding an identifier "TO IFA" and a lead line from the identified to node "B". Applicants also propose adding a "Clock Generation" box with identified output signals CTL_SAZ, CTL_SBZ, CTL_D, and CTL_P. The timed operation of switches to combine and split capacitors is described in the specification on page 6, lines 17-29. LO is shown in Figure 4A and in US 2003/0034499 A1, which is incorporated by reference. The output connected to IFA input is shown also in Figure 4B.

Applicants respectfully request approval.

Respectfully submitted,



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